

# 74ABT2244

## Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

### Features

- Guaranteed latching protection
- High-impedance, glitch-free bus loading during entire power up and power down cycle
- Nondestructive, hot-insertion capability

### General Description

The ABT2244 is an octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

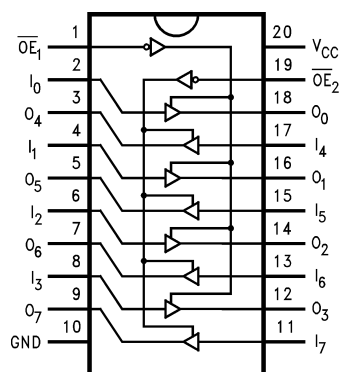
The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

### Ordering Information

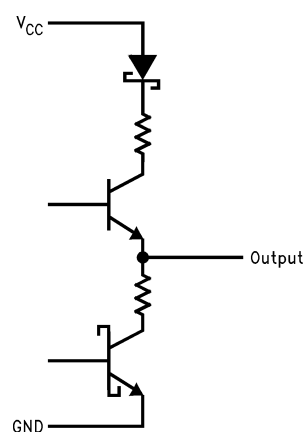
Order Number	Package Number	Package Description
74ABT2244CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ABT2244CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT2244CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ABT2244CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices are also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number. Pb-Free package per JEDEC J-STD-020B.

### Connection Diagram



### Schematic of Each Output



### Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active LOW)
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

### Truth Table

$\overline{OE}_1$	$I_{0-3}$	$O_{0-3}$	$\overline{OE}_2$	$I_{4-7}$	$O_{4-7}$
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level Z = High Impedance

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_A$	Ambient Temperature Under Bias	-55°C to +125°C
$T_J$	Junction Temperature Under Bias	-55°C to +150°C
$V_{CC}$	$V_{CC}$ Pin Potential to Ground Pin	-0.5V to +7.0V
$V_{IN}$	Input Voltage <sup>(1)</sup>	-0.5V to +7.0V
$I_{IN}$	Input Current <sup>(1)</sup>	-30mA to +5.0mA
$V_O$	Voltage Applied to Any Output Disabled or Power-off State	-0.5V to 5.5V
	HIGH State	-0.5V to $V_{CC}$
	Current Applied to Output in LOW State (Max.)	twice the rated $I_{OL}$ (mA)
	DC Latchup Source Current (Across Comm Operating Range)	-300mA
	Over Voltage Latchup (I/O)	10V

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$T_A$	Free Air Ambient Temperature	-40°C to +85°C
$V_{CC}$	Supply Voltage	+4.5V to +5.5V
$\Delta V / \Delta t$	Minimum Input Edge Rate	
	Data Input	50mV/ns
	Enable Input	20mV/ns

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input HIGH Voltage		Recognized HIGH Signal	2.0			V
V <sub>IL</sub>	Input LOW Voltage		Recognized LOW Signal			0.8	V
V <sub>CD</sub>	Input Clamp Diode Voltage	Min.	I <sub>IN</sub> = -18mA			-1.2	V
V <sub>OH</sub>	Output HIGH	Min.	I <sub>OH</sub> = -3mA	2.5			V
			I <sub>OH</sub> = -32mA	2.0			
V <sub>OL</sub>	Output LOW Voltage	Min.	I <sub>OL</sub> = 15mA			0.8	V
I <sub>IH</sub>	Input HIGH Current	Max.	V <sub>IN</sub> = 2.7V <sup>(3)</sup>			1	μA
			V <sub>IN</sub> = V <sub>CC</sub>			1	
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	Max.	V <sub>IN</sub> = 7.0V			7	μA
I <sub>IL</sub>	Input LOW Current	Max.	V <sub>IN</sub> = 0.5V <sup>(3)</sup>			-1	μA
			V <sub>IN</sub> = 0.0V			-1	
V <sub>ID</sub>	Input Leakage Test	0.0	I <sub>ID</sub> = 1.9μA, All Other Pins Grounded	475			V
I <sub>OZH</sub>	Output Leakage Current	0-5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}n = 2.0V$			10	μA
I <sub>OZL</sub>			V <sub>OUT</sub> = 0.5V; $\overline{OE}n = 2.0V$			-10	
I <sub>OS</sub>	Output Short-Circuit Current	Max.	V <sub>OUT</sub> = 0.0V	-100		-275	mA
I <sub>CEX</sub>	Output HIGH Leakage Current	Max.	V <sub>OUT</sub> = V <sub>CC</sub>			50	μA
I <sub>ZZ</sub>	Bus Drainage Test	0.0	V <sub>OUT</sub> = 5.5V, All Others GND			100	μA
I <sub>CCH</sub>	Power Supply Current	Max.	All Outputs HIGH			50	μA
			All Outputs LOW			30	
I <sub>CCZ</sub>	Power Supply Current	Max.	$\overline{OE}n = V_{CC}$ , All Others at V <sub>CC</sub> or GND			50	μA
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input	Max.	Outputs Enabled	V <sub>I</sub> = V <sub>CC</sub> - 2.1V		2.5	mA
			Outputs 3-STATE	Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V		2.5	
			Outputs 3-STATE	Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V, All Others at V <sub>CC</sub> or GND		50	
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> No Load <sup>(3)</sup>	Max.	Outputs OPEN, $\overline{OE}n = GND^{(2)}$ , One-Bit Toggling, 50% Duty Cycle			0.1	mA/MHz

## Notes:

1. Either voltage limit or current limit is sufficient to protect inputs.
2. For 8-bit toggling, I<sub>CCD</sub> < 0.8mA/MHz.
3. Guaranteed, but not tested.

## AC Electrical Characteristics

SOIC and SSOP packages.

Symbol	Parameter	$T_A = +25^\circ\text{C}$ , $V_{CC} = +5\text{V}$ , $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $V_{CC} = 4.5\text{V} - 5.5\text{V}$ , $C_L = 50\text{pF}$		Units
		Min.	Typ.	Max.	Min.	Max.	
$t_{PLH}$	Propagation Delay, Data to Outputs	1.0	2.2	3.9	1.0	3.9	ns
$t_{PHL}$		1.0	2.9	4.4	1.0	4.4	
$t_{PZH}$	Output Enable Time	1.5	3.7	6.0	1.5	6.0	ns
$t_{PZL}$		2.1	4.3	7.0	2.1	7.0	
$t_{PHZ}$	Output Disable Time	1.7	3.5	5.8	1.7	5.8	ns
$t_{PLZ}$		1.7	3.7	5.8	1.7	5.8	

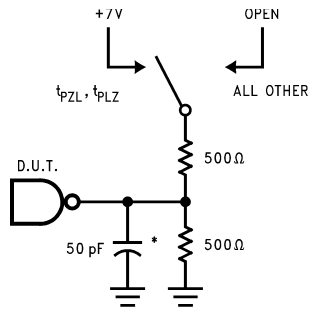
## Capacitance

Symbol	Parameter	Conditions ( $T_A = 25^\circ\text{C}$ )	Typ.	Units
$C_{IN}$	Input Capacitance	$V_{CC} = 0\text{V}$	5.0	pF
$C_{OUT}^{(4)}$	Output Capacitance	$V_{CC} = 5.0\text{V}$	9.0	pF

**Note:**

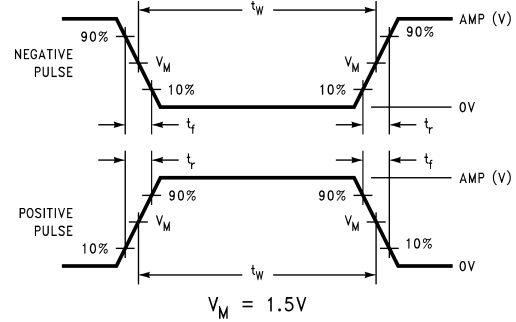
4.  $C_{OUT}$  is measured at frequency  $f = 1\text{MHz}$ , per MIL-STD-883, Method 3012.

### AC Loading



\*Includes jig and probe capacitance

**Figure 1. Standard AC Test Load**

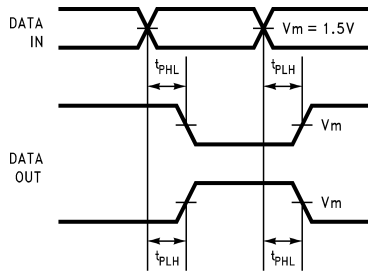


**Figure 2. Test Input Signal Levels**

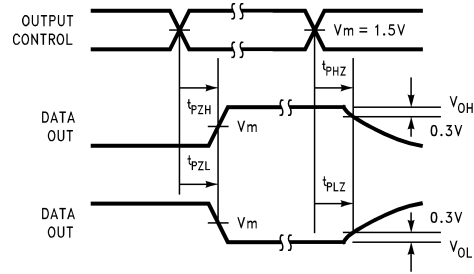
Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1MHz	500ns	2.5ns	2.5ns

**Figure 3. Test Input Signal Requirements**

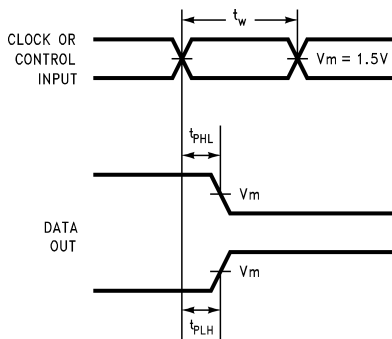
### AC Waveforms



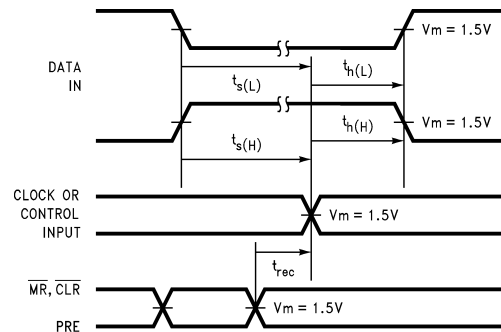
**Figure 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**Figure 5. 3-STATE Output HIGH and LOW Enable and Disable Times**



**Figure 6. Propagation Delay, Pulse Width Waveforms**



**Figure 7. Setup Time, Hold Time and Recovery Time Waveforms**

## Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

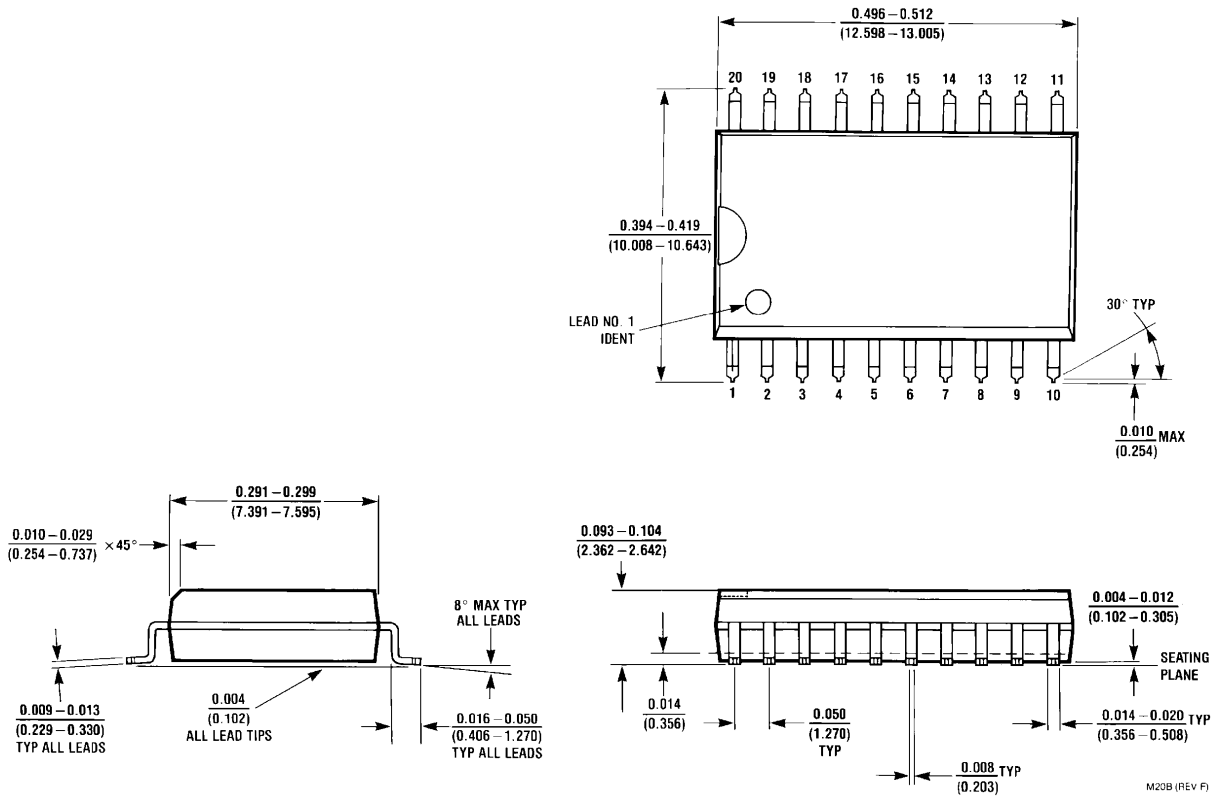
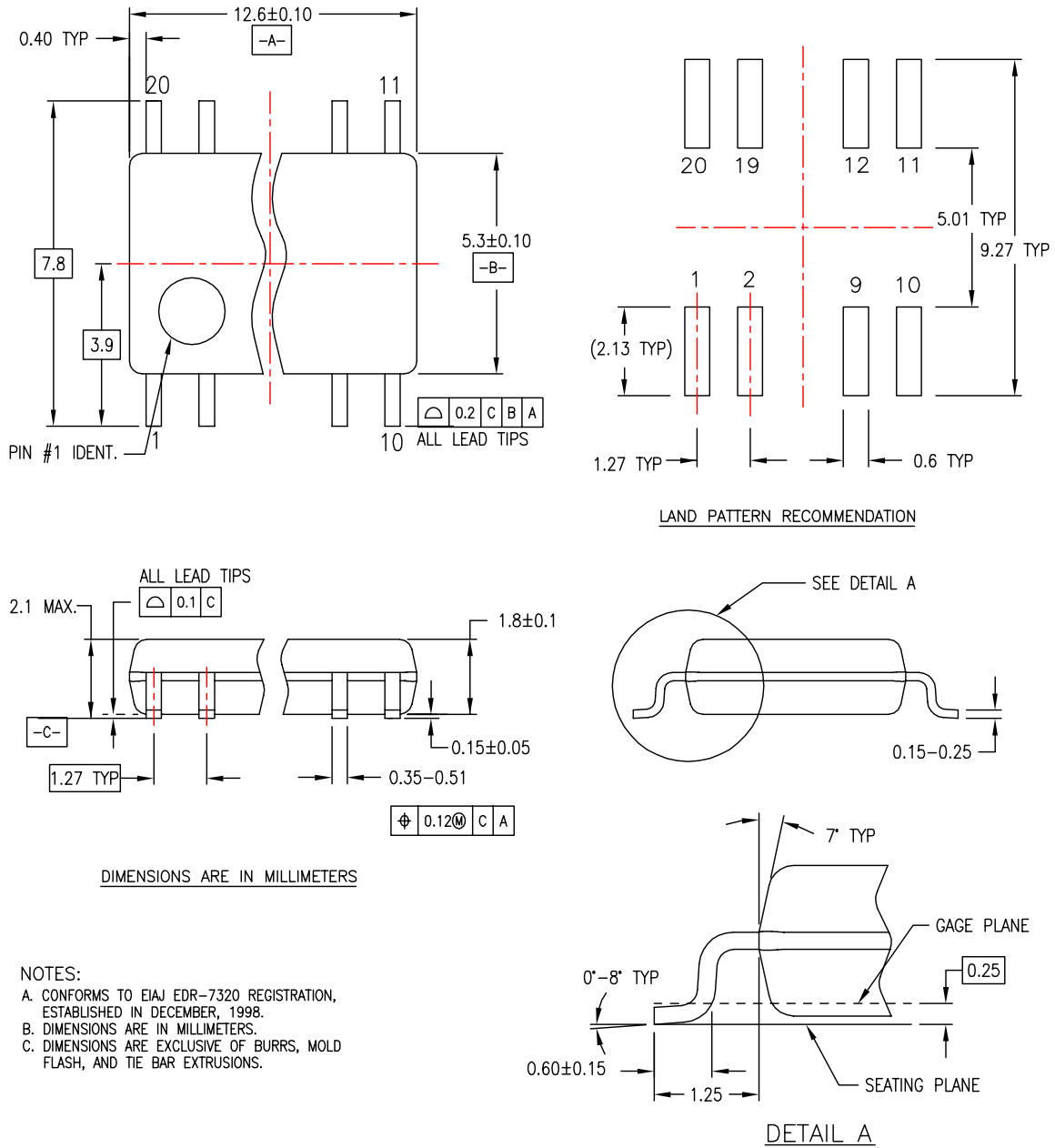


Figure 8. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

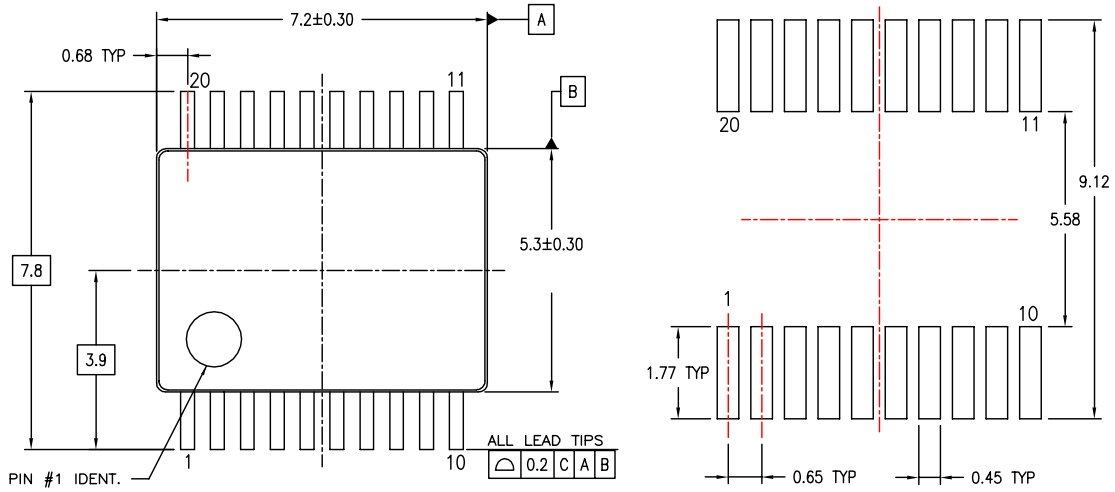
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

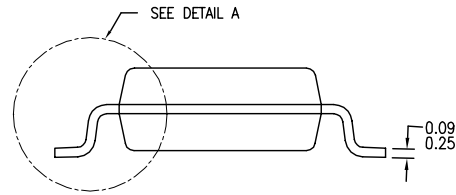
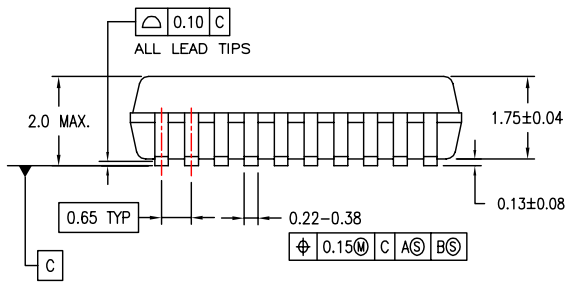
**Figure 9. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D**

### Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



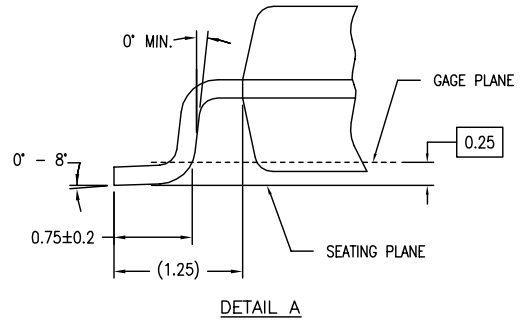
#### LAND PATTERN RECOMMENDATIONS



DIMENSIONS ARE IN MILLIMETERS

#### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-150, VARIATION AE, DATE 1/94.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M - 1994.



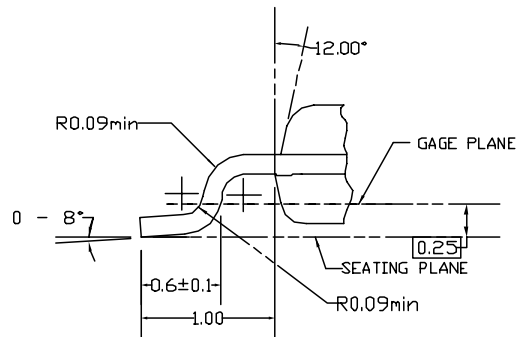
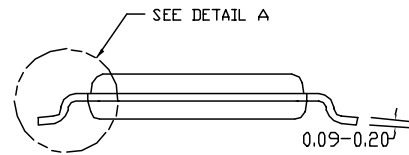
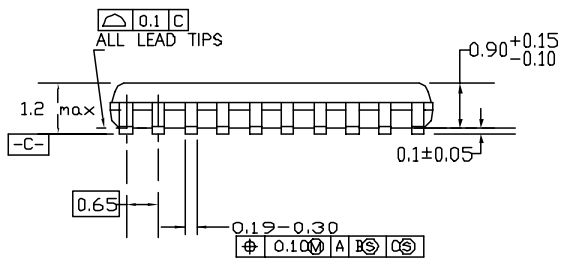
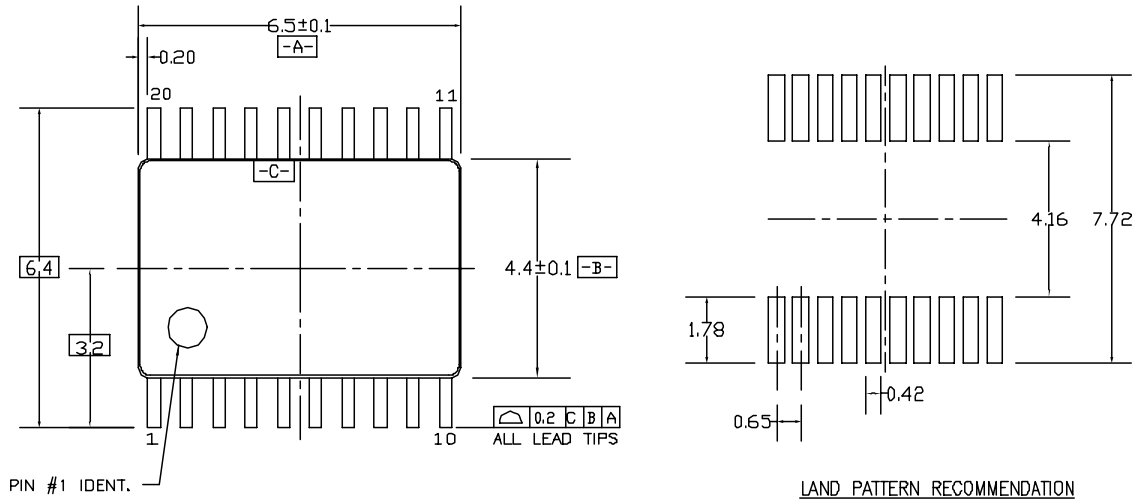
MSA20REVB

**Figure 10. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide Package Number MSA20**



**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.


MTC20REV D1

**Figure 11. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**



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Datasheet Identification	Product Status	Definition
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